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PATENT
005586-20026 (81784.0018)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Akira TSUKIHASHI

Serial No: 09/476,862

Filed: January 3, 2000

For: DATA PROCESSING CIRCUIT FOR TEMPORARILY SUSPENDING DATA RECORDING ONTO A DISK (As Amended)

Art Unit: 2655

Examiner: G. Patel

ABrief
8403

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07/23/03
Signature Date

APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal from the Examiner's Final Rejection of claims 3-12. The Final Rejection issued on April 9, 2003 and the Notice of Appeal was received in the Patent and Trademark Office on July 11, 2003.

REAL PARTY IN INTEREST

The real party in interest is Sanyo Electric Co., Ltd., Osaka, Japan.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 3-12 are pending. This Appeal is directed to the final rejection of claims 3-12.

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STATUS OF AMENDMENTS

A Response to Final Office Action was filed on May 19, 2003, and an Advisory Action issued on May 28, 2003 in response thereto.

SUMMARY OF INVENTION

This invention relates to a recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a non-erasable, write-once disk.

Conventional data recording devices, such as CD-R drives and CD-RW drives, record data onto an optical disk. Oftentimes, the data recording device may have a high-speed writing capability and can record data onto the disk at a speed faster than the speed at which it receives data from an external source. As a result, data writing by such data recording device is often performed intermittently, resulting in waste of power.

The present invention provides a recording data processing device with a data processing circuit for recording data onto a disk, a control circuit controlling the data processing circuit for writing and/or reading data to and from the disk, and a buffer memory for temporarily storing the data to be recorded onto the disk or reproduced from the disk. In one aspect of the invention, the control circuit controls data reading from or recording onto the disk based on the amount of data having been stored in the buffer memory. The control circuit suspends operation of the data processing circuit by either interrupting the power supply or by halting the supply of an operation clock supplied to the data processing circuit until the data stored in the buffer memory reaches a predetermined amount. As a result, the recording data processing device according to the invention reduces its power consumption when recording and/or reproducing data onto/from the disk. This is described, for example, at line 24 of page 6 through line 4 of page 8 of the application, and at lines 16-21 of page 16 of the application. In accordance with another aspect of the invention, in resuming the recordation of data on the disk, the

recording device synchronizes the new data about to be recorded onto the disk and the data previously recorded on the disk immediately before the discontinuation of data recording. Therefore, the new recording data can be recorded in a region on the disk successive, and without a break, to a region where the last recording data was recorded immediately before the discontinuation of data recording. This is described at line 23 of page 11 through line 5 of page 12 of the specification.

Therefore, unlike certain systems of the prior art as discussed hereafter, in devices according to the present invention, the data to be recorded, which is output from an encoder, is synchronized to data already recorded onto the disk in order to allow additional recording continuously from a position so that there is no gap from the data recorded immediately before suspension of recording. This is described at line 23 of page 11 through line 5 of page 12 of the specification.

Also, and as contrasted with certain systems of the prior art discussed hereafter, the operation of a data processing circuit in accordance with the invention is placed in a suspended state by interrupting the power supply to the data processing circuit or by halting the supply of a data clock to the data processing circuit. Consequently, power consumption can be reduced. It is not a feature of the present invention to simply interrupt the operation when there is no data.

ISSUES

The issue to which this Appeal relates is whether the recording data processing device defined in the claims on Appeal is unpatentable over U.S. Patent 5,436,875 of Shinada in view of U.S. Patent 5,434,997 of Landry.

GROUPING OF CLAIMS

The rejected claims stand or fall together.

ARGUMENT

In rejecting the claims as unpatentable over Shinada in view of Landry, the Final Office Action purports to show the manner in which Shinada and Landry disclose or suggest the various limitations of the claims. Beginning with paragraph 15 on page 9 of the Final Office Action, Applicant's argument set forth in the Remarks section of the prior amendment are discussed in terms of why such arguments are incorrect or not persuasive.

Various statements and arguments set forth in the Final Office Action with respect to the Shinada and Landry references are fundamentally incorrect. More particularly, and in the case of Shinada, it is stated in the Final Office Action that the ROM (read-only-memory) referred to in Shinada includes a "write-once" media. However, the disc of Shinada is a CD (compact disc) which is used for reproduction only. Nowhere does Shinada disclose that such disc is writable.

Shinada describes a first embodiment (Fig. 1) which uses a hybrid device for reading and writing. Shinada also discloses a second embodiment (Fig. 8) and a third embodiment (Fig. 13). The second and third embodiments use a combination of a reproduction-only disk and a writable disk. The reproduction-only disk is a music CD in which no writing is performed. With the description "reproduction-only" being used in the specification, it is very clear that the disk is not a CD-R.

Moreover, Shinada does not disclose or suggest generating a reproduction clock and operating in synchronization with such clock.

Regarding the Landry patent, such reference describes that the slave CPU is put into a sleep state when the data on the bus is not for the CPU. The present invention differs from Landry. In the case of the present invention, operation is suspended by interrupting the power supply or halting the supply of an operation clock when buffer underrun occurs.

Therefore, claims 3-12 are submitted to clearly distinguish patentably over the attempted combination of Shinada and Landry.

In the case of claim 3, for example, such claim defines a recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data "onto a non-erasable, write-once disc". The circuit is comprised of a buffer memory, a data processing circuit, a system control circuit, and a writing circuit. The system control circuit is said to suspend operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in a buffer memory, and to release suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory. The data processing circuit for recording data is placed in a suspended state "by interrupting the power supply or by halting the supply of an operation clock". Further, the system control circuit "stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address". Still further, the system control circuit "synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk". As described in detail above, the cited references do not show or suggest, taken alone or in the attempted combination thereof, such a recording data processing circuit in accordance with the invention.

Similar comments apply to independent claim 7 which defines a recording data processing circuit in similar fashion, and to claims 4-6 and 8-12 which depend from and contain all of the limitations of their parent claims.

In conclusion, claims 3-12 are submitted to clearly distinguish patentably over the cited art for the reasons set forth above. It is therefore respectfully

requested that the final rejection of the claims be reversed and that claims 3-12 be determined to be allowable.

The present Brief is submitted herewith in triplicate along with an Appendix containing the appealed claims and the requisite brief fee.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: July 23, 2003

By: _____
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

APPENDIX: CLAIMS 3-12 ON APPEAL

3. A recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a non-erasable, write-once disk, comprising:

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory;

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit, and

a writing circuit for writing the recorded data supplied from the data processing circuit, onto the disk,

wherein

the system control circuit suspends operation of the data processing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit for recording data being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock,

wherein

the system control circuit stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address,

and wherein

the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being

operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.

4. A recording data processing device according to claim 3, further comprising a motor control circuit for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended, at a same speed as that at which the disk rotated immediately before the suspension of data recording.

5. A recording data processing device according to claim 3, wherein the writing capacity of the buffer memory is set at full memory capacity of the buffer memory.

6. A recording data processing device according to claim 3, wherein the writing capacity of the buffer memory is set at full memory capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed.

7. A recording data processing circuit for processing received data sent at a slower data transmission speed than a data processing speed at which to write recording data onto a disk, and recording the recording data onto the disk, comprising:

a buffer memory for temporarily storing the received data;

a data processing circuit for preparing the recording data to record onto the disk, based on the received data read from the buffer memory;

a system control circuit for controlling writing and reading of the received data with respect to the buffer memory, and operation of the data processing circuit, and

a writing circuit for writing the recording data supplied from the data processing circuit onto the disk,

wherein

the system control circuit suspends operation of the data processing circuit and writing of the recording data onto the disk by the writing circuit until an amount of received data equivalent to a predetermined writing capacity has been stored in the buffer memory, and releases suspension of the operation of the data processing circuit to resume writing of the recording data onto the disk by the writing circuit when an amount of received data equivalent to the predetermined writing capacity has been stored in the buffer memory, said data processing circuit being placed in a suspended state by interrupting the power supply or by halting the supply of an operation clock.

8. A recording data processing circuit according to claim 7, wherein the system control circuit stores an address successive to an address of received data last recorded onto the disk, as a recording start address on the disk, and controls the writing circuit so as to write the recording data supplied from the data processing circuit onto the disk at the recording start address.

9. A recording data processing device according to claim 8, wherein the system control circuit synchronizes the recording data to be newly recorded onto the disk, supplied from the data processing circuit to the writing circuit, with recording data recorded on the disk, said data processing circuit being operated in synchronism with a reproduction clock obtained by reproducing the data already recorded on the disk.

10. A recording data processing device according to claim 9, further comprising a motor control circuit for controlling a motor for driving the disk, wherein the motor control circuit controls the motor such that the disk rotates, while operation of the data processing circuit is suspended, at a same speed as that at which the disk rotated immediately before the suspension of data recording.

11. A recording data processing device according to claim 9, wherein the writing capacity of the buffer memory is set at full memory capacity of the buffer memory.

12. A recording data processing device according to claim 9, wherein the writing capacity of the buffer memory is set at full memory capacity of the buffer memory deducted by an amount of data expected to be written into the buffer memory before data recording onto the disk is resumed.